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Reliable Low-Power Design in the Presence of Deep Submicron Noise Naresh Shanbhag Coordinated Science Lab ECE Department University of Illinois at

M. Laurent, M. Briet, Low Power Design Flow and Libraries , in NATO ASI Series Low Power Design in Deep Submicron Electronics , Kluwer Academic Publishers  
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Voltage Technologies, Low Power Design (1997) by C Venue: in Deep Submicron Electronics (NATO Asi Series. Series E, Applied Sciences, Vol 337: Add To MetaCart.

Low Power Dynamic Bus Encoding for Deep Sub-micron Design Kun-Lin Tsail Department of EE1 National Taiwan University Taipei 106, Taiwan. kunlin@orchid.ee.ntu.edu.tw

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UNIT II LOW POWER DESIGN 9 Sources of CMOS power consumption-technology options for low power-reduction of P-leak Low Power Design in Deep Submicron Electronics

Software design for low power, in Low power design in deep submicron electronics (1997)

Language English. Imprint Dordrecht ; Boston : Kluwer Academic Publishers, c1997. Physical description xvi, 580 p. : ill. ; 25 cm. Series NATO ASI series.

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